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Materials Technologies for Thermomechanical Management of Organic Packages

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Index words: thermomechanical stress, underfill, barrier layer metallization, thermal interface material, molding compound

ABSTRACT

Microelectronic package materials must be designed to enable the electrical and thermal performance requirements and to provide high-reliability performance in order to keep pace with silicon and package technology advances. One key challenge for high-reliability performance is the warpage and thermomechanical stresses that organic packages experience upon changes in temperature and/or relative humidity due to the mismatch in the Thermal Expansion Coefficient (CTE) between the die and the organic substrate. In this paper, we show three examples of materials technologies developed to enable low stress and low warpage organic packages: (1) first-level interconnect Underfill (UF) and barrier layer metallization for organic flip-chip packages, (2) Thermal Interface Material (TIM) for heat removal, and (3) molding compound for wirebonded dies in a new stacked package form factor.

One of the key challenges faced by solders is their performance in reliability tests. These materials are susceptible to thermal fatigue under accelerated tests. The main function of the UF is to protect the interconnect from solder fatigue failure that arises from thermomechanical stresses. In addition, the properties of the UF should be such that they do not impart other stresses on the bump during thermal cycling. This requires carefully controlling the mechanical, thermal, and adhesion properties of the UF. Moreover, understanding the interaction of the PbSn solder with the barrier layer metallization on the die is key to achieving good reliability performance.

Silicone gel TIMs were developed for high-performance, high-power processors that require the use of integrated heat spreaders. In addition to transferring heat, the TIM must also dissipate thermomechanical stresses resulting from the mismatch of thermal expansion between the different materials. Low modulus materials provide the desired stress relief and also exhibit improved heat removal due to reduced interfacial resistance. However, if the modulus of the TIM is too low, then reliability issues, such as pump-out, are observed. The optimum modulus was achieved in our application by chain extension technology, which provided modulus control over a wide range of values.

The folded stacked chip scale package is a key next-generation package technology that was developed to integrate multiple memory and logic chips into a single module. This package technology involves package stacking as well as die stacking. The key challenge for the Folded Stacked Chip Scale Package (FSCSP) mold compound was achieving the tight warpage target of 20 microns, required to enable folding and package stacking. This challenge was met by increasing the amount of silicone modifier in the mold compound.

INTRODUCTION

The microelectronic package continues to evolve to improve performance and integrate new technologies, such as fragile silicon dielectric layers, multicore and multidie architectures, thinner substrates, increasing integration of passive components, increasing thermal design power, and lead-free interconnects [1]. Package

materials must also keep pace with silicon and package technologies. They must be designed to enable the electrical and thermal performance requirements and to provide high-reliability performance. One key challenge for high-reliability performance is the warpage and thermomechanical stresses that organic packages experience upon changes in temperature and/or relative humidity due to the mismatch in the Thermal Expansion Coefficient (CTE) between the die at about 3ppm/°C and the organic substrate at about 20ppm/°C. There is a wide variety of materials used for microelectronic device packages, and the material type, function, and thermomechanical performance requirements depend on the package form factor. In this paper we examine three examples of materials technologies developed to enable low-stress and low-warpage microelectronic packages.

FIRST-LEVEL INTERCONNECT

The primary roles of solder materials in flip-chip electronic packages is to enable the interconnection between the die and the package, which is called the First-Level Interconnect (FLI), and to enable the interconnection between the package and motherboard, which is called the Second-Level Interconnect (SLI). Both of these types of interconnections allow a high density of input/output connections, ensure maximum usage of die and package real estate, and allow relative ease of scalability to finer pitches.

The melting temperature of the FLI solder needs to be high enough to maintain integrity during subsequent assembly processes such as epoxy curing and package-to-board mounting. To satisfy this boundary condition, high Pb solders with a liquidus of 320°C are used (95Pb-5Sn) as die side bumping solders. These solders are reflowed above the melting temperatures to directly bond the die to the ceramic substrate. The drive to reduce the cost of the packages in high-volume manufacturing saw the advent of thermoset organic packages to replace ceramic packages. The inability of the organic packages to withstand temperatures greater than about 300°C necessitated the use of eutectic PbSn solders (63Sn-37Pb) on the package side to enable the chip attach. The eutectic PbSn solder melts at 183°C and lends itself extensively to high-volume manufacturing. One of the key advantages of using the high Pb die bump and eutectic PbSn substrate solder is the substantial reduction of thermomechanical stresses on the Interlayer Dielectric (ILD) layers utilized in the 90nm silicon backend technology. There are several additional advantages of the eutectic PbSn solder approach, namely the high compliancy of the solder, the ability of the chip and the substrate to self-align during reflow, the interdiffusion of the solders without the formation of Intermetallic Compounds (IMCs) in the solder joints, and the ability to achieve consistent stand-off height.

A typical organic package is expected to withstand temperature cycling and humidity stresses [2]. The reliability stressing is used to assess the package performance in an accelerated fashion to extrapolate the lifetime that may be expected under normal operating conditions. Bump fatigue cracking is caused by cyclic application of shear stress to the interconnect bump during temperature cycling due to mismatch between the CTE of the die, solder interconnect, and substrate, which is represented in Figure 1. The utilization of high-lead die bump and eutectic PbSn substrate solder joint significantly reduced the risk of excessive stress transfer to the ILD but brought new challenges with the integration of a high-temperature wafer reflow process and the associated impacts to barrier layer metallization delamination.

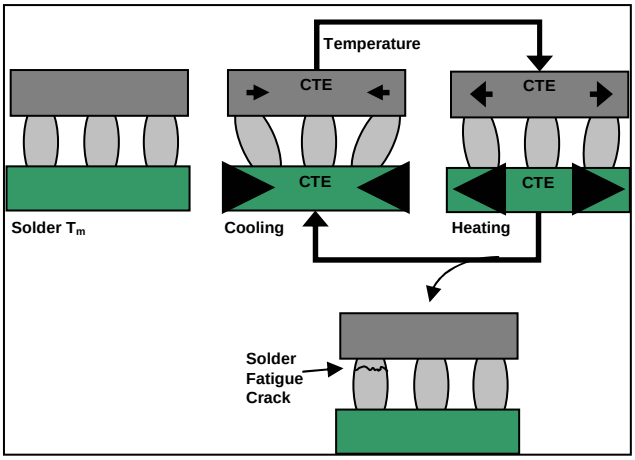

Figure 1: Schematic of package in reliability stress illustrating CTE mismatch

Underfill

The main function of the UF is to protect the interconnect from solder fatigue failure that arises from mechanical stress induced during temperature cycling due to the CTE mismatch between the silicon die, the interconnect solders, and the organic substrate. The UF distributes the shear stresses over the entire area of the die thereby reducing the stress on individual bumps. The mechanical properties of the UF that are critical for distributing shear stress are modulus,CTE and T_g.

Although the UF protects the bump from shear stresses, the properties of the UF should be such that it, the UF, does not impart other stresses on the bump or the die during thermal cycling. Thus, to prevent tensile and compressive stress fatigue cracking in the interconnect, the CTE of the UF should be similar to that of the interconnect metal, which is about 26ppm/°C for solder interconnect and lower (to 16ppm/°C) if a significant

portion of the interconnect metal is copper. In theory, UFs with CTE significantly higher or lower than these values would be likely to cause fatigue cracking in the flip-chip solder joints during temperature cycling. The maximum CTE of unfilled epoxy thermosets is about 60ppm/°C. Thus, to attain the target CTE, UFs are filled with silica, which has a CTE of 0.5ppm/°C.

The CTE of spherical silica-epoxy composites follow roughly a rule of mixture relationship; however, there is an influence from the interphase region between the matrix and the filler particles that can lead to deviation from linearity [3]. This interphase region which has mechanical properties that are different from those of the bulk matrix or filler has been directly observed by scanning force microscopy for polymer-fiber composites [4]. The CTE is also predicted to decrease with filler particle size at a given filler loading, but unfortunately the benefit of the interphase region tends to converge with the rule of mixing behavior at high filler loading.

Die cracking is a low temperature phenomenon, as can be determined by the occurrence of die cracking in temperature cycle tests that go to very low temperatures (i.e., -55°C) versus the lack of die cracking in temperature cycle tests that go to moderately low temperatures (-25°C). Figure 2 shows the "half-moon" shape of a typical die crack. Die cracking may or may not lead to electrical failure. The die crack phenomenon is due to a combination of factors, including the fillet angle (shown in Figure 2) and the modulus of the material at low temperature. A higher fillet angle and a higher modulus both lead to higher principle die stress at a given temperature, leading to a greater likelihood of die cracking. The fillet angle is determined in part by the processing conditions and in part by the rheology of the material.

It follows that the UF should have sufficient modulus to handle the stresses induced upon it. The lower limit for modulus in terms of protecting the bump is not rigorously known and depends on the particulars of the package; however, the modulus should be in the GPa range. The addition of silica filler can significantly increase the modulus of the UF. The modulus of an unfilled epoxy thermoset in the glassy state is approximately 2-4 GPa, whereas the addition of silica filler to 65-70% increases the modulus to about 9-15 GPa. Adding filler, however, has a profound effect on the rheology of the UF; hence, there are limitations on filler loading levels that can be achieved.

The influence of the modulus of the UF on package reliability is complex and critical. The modulus must be balanced between the extremes. A high UF modulus, while necessary to mitigate shear stresses and bump fatigue cracking, can lead to die cracking in reliability testing, especially for bare die packages, i.e., packages without an integrated heat sink mechanically coupled to the die [5].

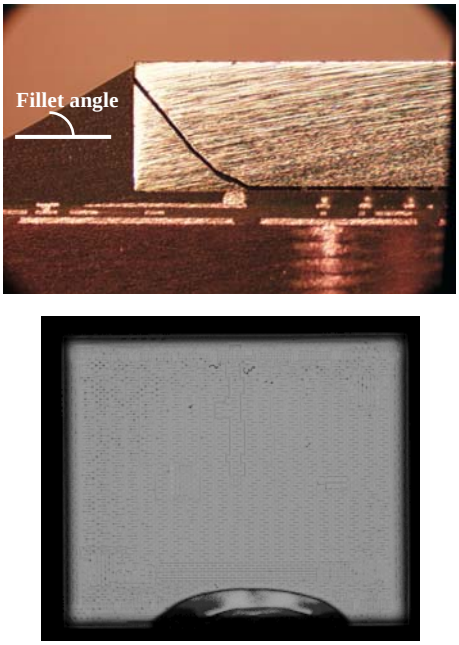

Figure 2: Illustration of die cracking in cross-section and CSAM

Low modulus UF is also a key technology for the protection of low- and ultra-low-K ILD in the upper routing layers of the die [6-9]. The mechanical sensitivity of low-K ILD materials is well documented. Typical ILD failure mechanisms are cracking near the edge of the die or under bump delamination. Both are caused by excessive stress on the die exacerbated by high modulus UF materials. For edge crack/delamination, it is critical that the UF edge coverage be sufficient and that there not be any voids or stress concentrators in the fillet region near the die edge. The fillet angle and shape, and other factors such as the chip attach process and flux, however, have substantial effects on the ILD performance. Therefore, an integrated engineering solution is required for robust packaged ILD silicon, one component of which is a low modulus and high glass transition temperature UF.

Formulating a lower modulus UF is typically accomplished by incorporating various types of rubber modifiers, as discussed above. The drawbacks to this strategy are the potential for an increase in CTE and viscosity and a decrease in the glass transition temperature. A more elegant solution is the use of resin and hardener technology that gives a lower intrinsic CTE and thus enables a reduction in the filler loading. A reduction in filler loading will lead to a reduction in

modulus and viscosity without affecting the glass transition temperature; and is thus consistent with the technical direction for UF. The challenge is that the CTE for organic materials is not very well understood and not predictable at this point, although some group contribution approaches have been documented [10]. New epoxy resins or new thermoset chemistries may be needed.

Low modulus also has negative ramifications on the reliability of the package. Bump fatigue was mentioned, but another phenomenon that can occur is damage to the Barrier Layer Metallization (BLM). The type of BLM is determined by the metallurgy of the interconnect and fab considerations. For high-lead bumps, a complex multilayer BLM is needed, whereas for copper interconnection the BLM is much simpler. The stress on the BLM is essentially a ratcheting mechanism through the solder bumps. This ratcheting stress must be dissipated by the UF, or else delamination within the BLM will be observed. Since the failure occurs during the high end of the temperature cycle, this indicates that the modulus of the UF must retain a high value at high temperatures; in other words, the glass transition temperature must be high. Many commercial UFs have T_g in the 60-90°C range. To avoid extensive BLM delamination for a sensitive BLM, however, the UF glass transition temperature must be high so that it can dissipate stress at high temperatures. If there is substantial filler settling, however, even high glass transition temperature materials can lead to BLM delamination due to the low modulus resin-rich region at the die interface.

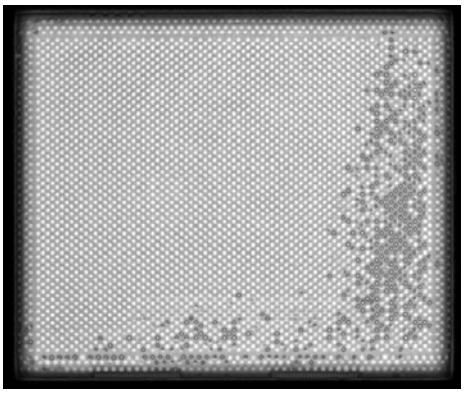

Figure 3: CSAM image showing presence of BLM delamination under the interconnect bumps

Another consistent reliability issue with UF materials is cracking. Cracking can take place at various locations and may or may not lead to electrical failure (Figure 4). The worst location for fillet cracking is at a die corner: cracks along the die edge typically do not propagate to the die or the substrate, whereas those at the corner can propagate to the substrate to break a copper trace, or they can spread underneath the die resulting in bump cracking (Figure 5).

Again, cracking is driven by stress, so the process conditions that give rise to the geometries of the fillet, etc. of the underfilled unit will determine the extent and effect of cracking. The fundamental mechanism of fillet cracking is not rigorously known. The hypothesis is that stress concentration at corner and edge locations leads to failure of the material. The root cause is likely related to low fracture toughness of thermosets; however, it could also be simply dictated by the material cohesive and/or adhesive strength.

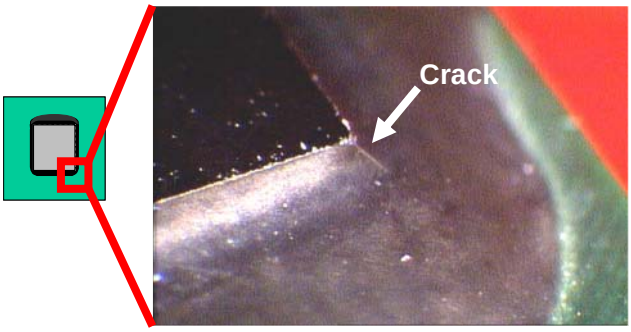

Figure 4a: Visual images of fillet crack in the underfill at a die corner

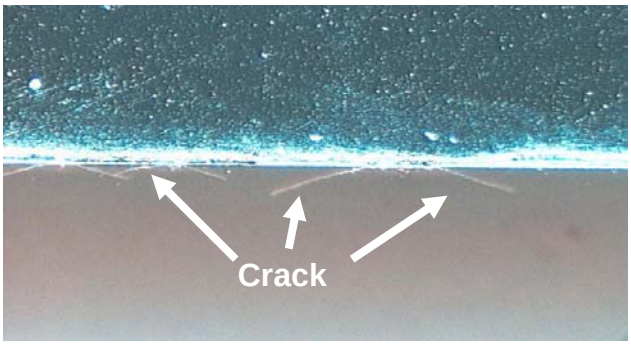

Figure 4b: Visual images of fillet cracks in the underfill along a die edge

The formulation aspects governing fracture toughness are not entirely well understood and the measurement of fracture toughness involves a relatively complex testing method. The use of higher molecular weight epoxy resins tends to result in thermosets with higher fracture toughness, by decreasing the crosslink density of the matrix. High molecular weight resins, however, also increase the viscosity of the material. Another very common method of toughening thermoset materials is the addition of liquid and solid rubber modifiers. The filler itself provides a significant increase in the fracture toughness due to the arresting of cracks at the filler surface, a well-known phenomenon in materials science. The filler distribution also plays a role in the fracture toughness, likely by increasing the probability that a crack will intersect a filler particle at an angle needed to arrest the crack. In general the presence of larger filler particles

will improve the fracture toughness [11, 12]; however, the largest filler size will still be limited by the chip-substrate gap height. Figure 5 shows the effect of toughener and filler on the fracture toughness of an UF.

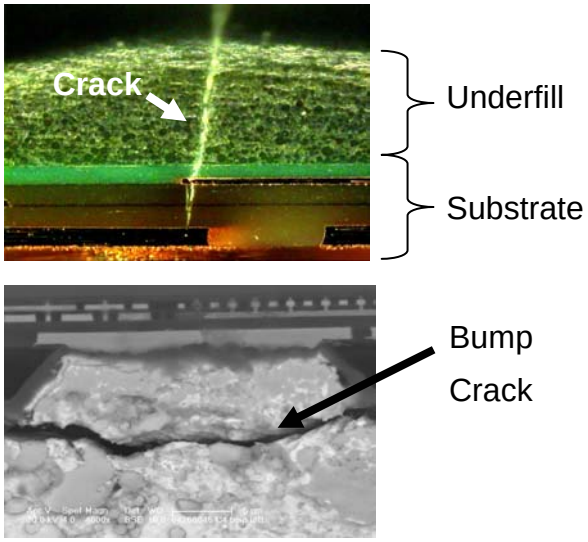

Figure 5: Fillet crack originates at the die edge and propagates resulting in cracking of the substrate Cu trace or propagates under the die resulting in bump cracking

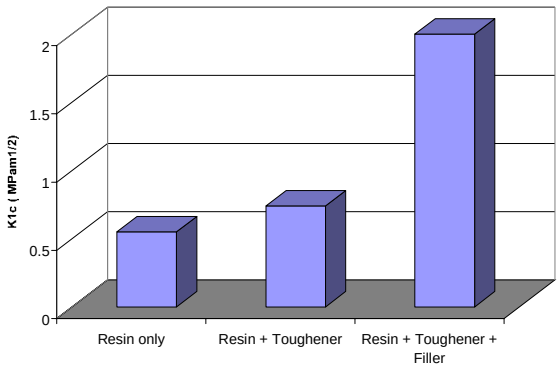

Figure 6: Impact of elastomer and elastomer + filler on fracture toughness of an underfill material

Delamination of UF at the die or substrate interface can occur during temperature cycling and humidity stress conditioning. Delamination during the temperature cycling is driven by stresses of a CTE mismatch between the die and the UF, due to both nominal and shear stresses. These stresses have been observed to be very high especially at the die edges, resulting in delamination at these areas. In fact, delamination is often observed to occur with fillet cracking (Figure 7).

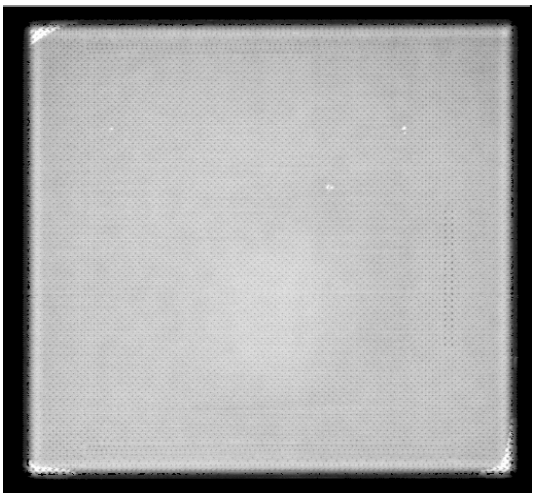

Figure 7: CSAM image showing corner delamination often observed with corner fillet cracks

Delamination of UF under moisture conditions can occur either at the UF-to-die passivation interface or at the UF-to-solder resist interface. Delamination of the UF can lead to solder bump fracture resulting in opens, or metal migration causing shorts under biased moisture conditions. Typically, delamination under moisture stress occurs due to poor adhesion of the UF at the interface of concern.

Adhesion of the UF to the interface is a combination of the physical contact to the surface and chemical bonds to the surface. The UF must wet the surface very well to form a good physical bond. The wetting characteristics are a function of temperature, so the temperature that the underfill and surface are subjected to during the process and during the beginning of the cure profile do affect the adhesion. The epoxy resin and hardener play a profound and not often predictable role in adhesion. Figure 8 shows the performance of two underfill formulations, one anhydride based and the other epoxy homopolymer based. As can been seen, although the anhydride-based underfill has very high adhesion post cure to the solder resist interface, post moisture exposure, the anhydride formulations are expected to drop in adhesion more sharply than epoxy homopolymer-based underfills. This phenomenon is fundamentally due to the ability of the anhydride-based formulations to pick up moisture, resulting in degradation of adhesion at the interface. A statistical approach with design of experiments is often the best known method for maximizing adhesion strength, although efforts to develop more predictive methods are underway. Coupling agents, usually trialkoxysilanes [13], are also added to formulations to form chemical bonds connecting the matrix and surfaces covalently. Typically epoxy functionalized trialkoxysilanes work well for the substrate surface, and amine coupling agents are useful for

the die passivation surface. Adhesion thus depends on the underfill formulation, the presence of reactive sites at the interface, and impurities at the substrate or passivation surface. Therefore the processing steps near the end of the substrate manufacturing process that affect the solder resist surface is important, as well as the processing of the die passivation layer. Furthermore, residues left over from the chip attach deflux process can dramatically affect the adhesion. The cure temperature and cure profile also affect the adhesion by not only modulating the formation of the physical bond to the substrate, as previously discussed, but also because of the chemical reactivity of the adhesion promoters. In general, adhesion test data must be gathered before and after moisture stress to understand the degradation of the adhesive bond and to predict and explain reliability performance. Mechanical shear tests are most often used to assess the adhesion strength to various surfaces, typically die shear, using 2x2mm die samples with appropriate passivation.

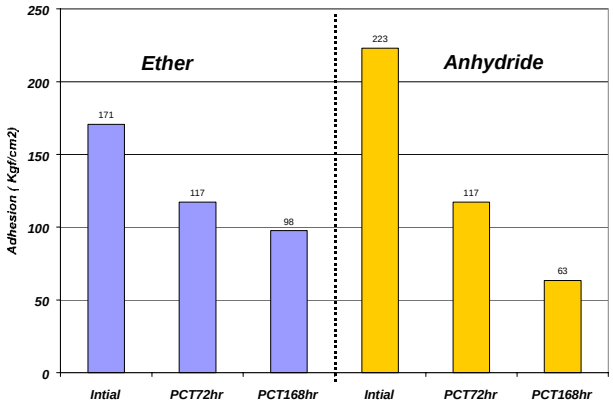

Figure 8: Button shear adhesion test indicating the impact of underfill material type of adhesion to solder resist post cure and post exposure to moisture stress

The Capillary Underfill (CUF) is the most mature and predominant UF technology that involves the use of capillary flow phenomena: this is where a liquid UF material fills the narrow gap between die and substrate via capillary action. Tailoring the material properties to mitigate the thermomechanical and processability requirements could be challenging. Other UF technologies that provide elegant ways of designing and processing UF materials consist of No Flow Underfill (NUF) and Over Molded Underfill (OMUF). NUF provides some unique package and silicon stress (BLM, ILD stress) mitigation opportunities by curing the material prior to package cool down from processing condition. As OMUF involves a molding compound transfer molding approach to underfill the FC die, the OMUF material thermomechanical properties could be tailored more easily than for CUF in terms of increasing filler content, modifying polymer resin chemistry, etc., because OMUF is not bound by capillary flow process boundary conditions.

Barrier Layer Metallization

One of the key challenges faced by FLI solders is the performance in reliability tests especially thermal fatigue under accelerated tests. Packages are subjected to a suite of accelerated reliability tests including a high-temperature bake, highly accelerated stress test (HAST) under humidity, and temperature cycling (TC-B) from 125 to -25°C [2]. The interaction of the PbSn solder with the Barrier Layer Metallization (BLM) on the die results in severe thermomechanical reliability failures. BLM performs several key functions in the C4 FLI. It forms a metallurgical bond between the die bump solder and the chip. The barrier layers also prevent the breaching of the Cu interconnect metal layers in the die with the Sn in the solders to form Cu-Sn Intermetallics (IMC). Additionally, the BLM provides electrical continuity between the chip and the package.

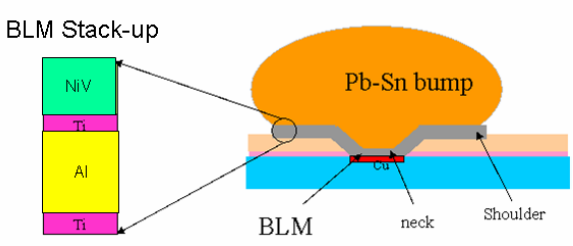

Figure 9: BLM stack-up for Pb-Sn bumps

The BLM stack-up shown in Figure 9 consists of Ti and NiV layers beneath the PbSn die bump. Analysis of the failure modes showed that the BLM delamination frequently occurred when the Ni diffused into the PbSn die bump forming a NiSn IMC leaving behind a porous vanadium-rich layer and Pb-rich regions in the bump. Two failure modes were seen for the BLM delamination: (1) cracking of the vanadium-rich layer and (2) delamination at the interface of the Ti/NiV to the lead-rich regions. Cross-section images of these fail modes are shown in Figures 10 and 11.

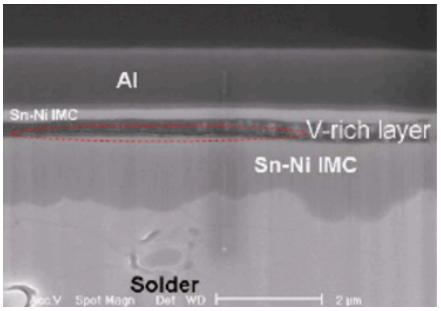

Figure 10: BLM delamination due to V-rich layer cracking

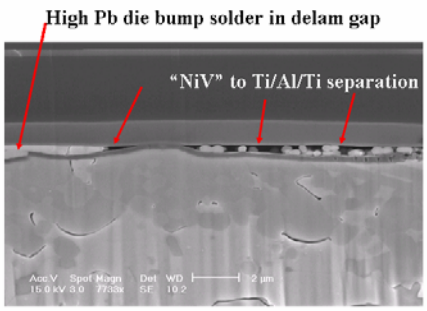

Figure 11: BLM delamination due to cracking of the V-rich layer

A reexamination of the assembly process flow and microstructure characterization showed significant consumption of the nickel in the BLM to form the Ni-Sn IMC during the initial wafer reflow process used to reflow the die-side 97Pb-3Sn bumps post electro-plating. In order to understand the BLM delamination failures, the thermodynamics and kinetics of the Ni-Sn IMC formation were evaluated as a function of wafer reflow thermal exposure.

The growth of NiSn IMC is governed by the following equation:

$$h = h_o \exp(-{E_a}/{kT})t^{1/n}$$

where h is the IMC thickness at temperature T and at time t, h_o is the thickness constant, E_a is the activation energy in units of eV, k is the Boltzmann constant, and n is the time exponent. E_a, h_o and n are three constants in the above equation that need to be determined in order to predict the IMC growth for any reflow profile. Additionally, these constants, especially the activation energy, tend to be significantly different in the solid vs. liquid regime. Hence, it was imperative to determine these constants in both the liquid and solid regimes by running appropriate experiments.

A 3x3 matrix of reflow temperatures and times was constructed, and singulated die were subjected to these reflow conditions followed by careful microstructural analysis to characterize the IMC composition, thickness, and level of kirkendall voiding. Kirkendall voiding is a metallurgical phenomenon which occurs as a result of diffusivity differences between thermally migrating atoms. Excessive diffusion of a certain atomic species down a chemical potential gradient causes vacancy diffusion and condensation in the opposite direction leading to voiding and potential BLM delamination failures. It was observed that the IMC thickness and kirkendall voiding increased substantially as the reflow temperature increased from 330 to 400°C. From the failure analysis data, the growth kinetics parameters were determined for the Ni-Sn IMC, and they are shown in Table 1.

Table 1: NiSn IMC growth kinetics

Regime	h_o (nm/sec $^{1/n}$)	E_a (eV)	n
Solidus	8000-10000	0.15-0.20	4
Liquidus	1800-2100	0.08-0.12	4

The low values of activation energy point to potential defects in the BLM layer that could accelerate the kinetics of IMC formation resulting in thicker IMCs from defect-driven growth. There have been several studies in the literature that have addressed the growth kinetics of IMC formation in NiSn and CuSn systems [14-26]. The values of E_a tend to vary between 0.09 and 0.26 eV in the liquidus for NiSn and n values ranging from 1.85 to 8.33. The large variation in these values is caused by several factors, including reaction-limited vs. diffusion-limited growth, changes in IMC stoichiometry (Ni_3Sn_2 to Ni_3Sn_4), diffusion occurring in several different phases, and the dependence of apparent diffusivity on grain size and composition. Thus the values obtained for the IMC growth kinetics fall within what is observed in the data.

Packages assembled from the die were subjected to different reflow profiles, and BLM delamination failures were monitored post 4x precon and 500 TC-B cycles. As seen from the results shown in Figure 12, increasing the wafer reflow temperature increased BLM degradation, which resulted in higher BLM delamination post precon and post TC-B testing. With this fundamental understanding, the flip-chip process was optimized to resolve BLM delamination.

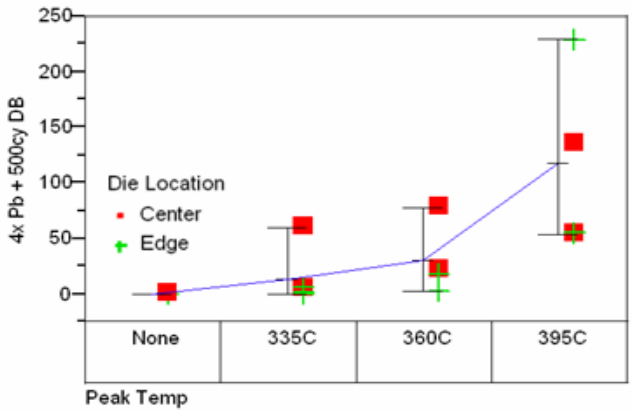

Figure 12: BLM delamination fails as a function of wafer reflow temperature

Extensive efforts are currently underway to provide Pb-free package solutions with the development of novel barrier layer metallizations and Pb-free FLI solder technology.

THERMAL INTERFACE MATERIAL

The primary role of thermal materials is to transfer the heat generated by the silicon die to the heat dissipation system, such as an air cooled heat sink. The recent trend in microprocessor architecture to meet the market demand for higher performance has resulted in the escalation of thermal design power and the heat flux at the silicon die [27]. As a result, a performance package was developed comprising a copper-based Integrated Heat Spreader (IHS) and a first-level TIM between the die and the heat spreader [28]. Consequently, the thrust for future improvement to meet the evolving thermal performance targets lies in the development of TIMs that can remove heat from the die to the IHS more effectively.

The metric used to identify thermal performance requirements and to select interface materials is the thermal resistance between the die and the heat sink described by the following equation [29]:

$$\theta_{jc} = \frac{T_j - T_c}{TDP} = R_{jc}(HF)$$

where T_j is the junction temperature at the active surface of the die, T_c is the temperature at the heat sink, *TDP* is the thermal design power, *HF* (heat flux) is the power dissipated per unit area, and R_{jc}, which typically has units of $^{o}Ccm^2/W$, is the thermal resistance normalized over a unit area. Based on the device design and the desired thermal performance, a target R_{jc} value of less than $0.25^{o}Ccm^2/W$ was established for the thermal solution for the flip chip ball grid array products. This represented a significant improvement in thermal performance, especially post reliability stressing.

A significant amount of theoretical understanding of the thermal resistance has been applied to the development of TIM formulations. The key TIM formulation development issues identified include bulk thermal conductivity, thermal interfacial resistance, and bond line thickness for package-level considerations and filler conductivity, filler loading, and filler particle size for material formulation considerations [29]. Optimizing thermal performance is achieved by manipulating these key parameters.

In addition, the TIM must be designed to manage the thermomechanical stresses in the package. As discussed in the previous section, upon cooling from the UF processing temperature, the die is curved due to the mismatch of the CTE between the die, the UF, and the substrate. This results in a certain amount of die stress that can be modeled by finite element analysis. As shown in Figures 13 and 14, the model predicts that when a high modulus TIM and copper IHS are used, the stress on the die increases significantly due to coupling of the die to the IHS rather than the substrate. When a low modulus TIM is used with a copper IHS, the natural curved shape of the die is maintained and the stress on the die is similar to the die stress observed without an IHS. Thus, based on the modeling results, the TIM material should have a low modulus.

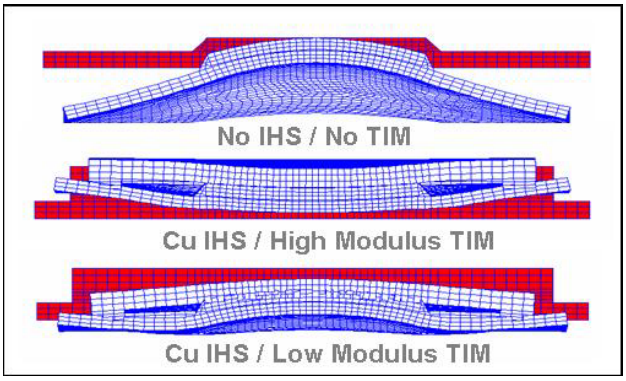

Figure 13: Finite element analysis results

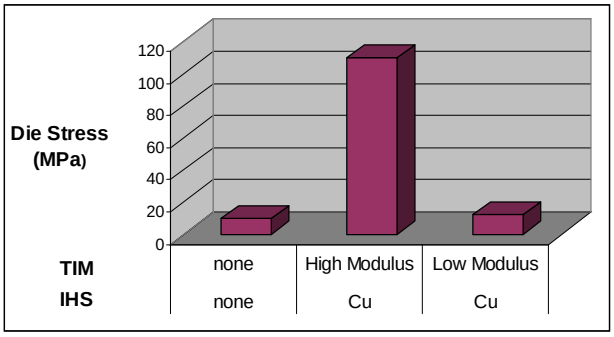

Figure 14: Die stress obtained from finite element analysis

Gel materials were developed for high-performance, high-power processors that require the use of IHSs [28]. Gels typically comprise a lightly crosslinked silicone polymer and a high loading of a conductive filler. The silicone resin is typically a vinyl-terminated silicone oil (shown in Figure 15) which is cured by hydrosilation using a silane hydride crosslinker (shown in Figure 16). The crosslinking reaction provides enough cohesive strength to circumvent the pump-out issues exhibited by greases during temperature cycling. Yet, their modulus is low enough (MPa range) that the material can still dissipate internal stresses and prevent interfacial delaminations. Thus, the low modulus properties of these filled gels are attractive from a materials integration standpoint.

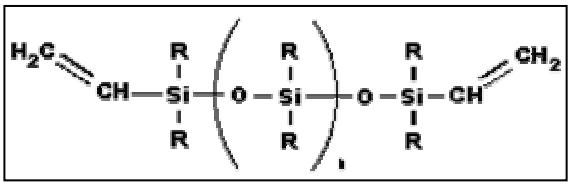

Figure 15: Chemical formula of a typical vinyl-terminated silicone oil

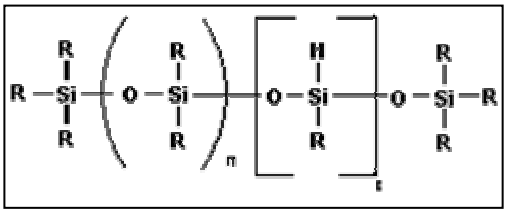

Figure 16: Chemical formula of a typical silicone oil crosslinker

As the package design evolves to achieve higher performance, the TIM must also evolve to achieve the optimum modulus value for the package design. Thus there is a need for methods to control the modulus of the gel TIM. There are several potential ways to control modulus. One very promising approach is to use a chain extender, which, as shown in Figure 17, is a low molecular weight hydrogen terminated silicone resin that forms linear polymer that reduces crosslink density. In addition to modulus control, chain extenders offer the potential to reduce the viscosity of the formulation to provide improved processibility. For this reason, the approach that was selected for modulus control involved the use of mixtures of chain extender and crosslinker.

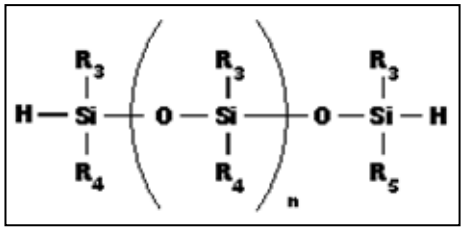

Figure 17: Chemical formula of a typical chain extender

A series of gel TIMs with increasing amounts of chain extender (measured as percent silane hydride from chain extender) and, therefore, decreasing amounts of crosslinker, were prepared. From the plot in Figure 18, it can be seen that by controlling the concentration of the chain extender, the modulus (G') measured by a Rhemetric Dynamic Analyzer can be controlled over a wide range of values (in this case the G' ranges from about 500 to about 1 kPa). One interesting observation is that at 80% and higher chain extender, the cured TIM no longer exhibits gelation as indicated by the crossover of the storage and loss modulus (G'/G" crossover). The lack of a G'/G" crossover point means that, after cure, TIMs comprising high chain extender concentrations remain greases.

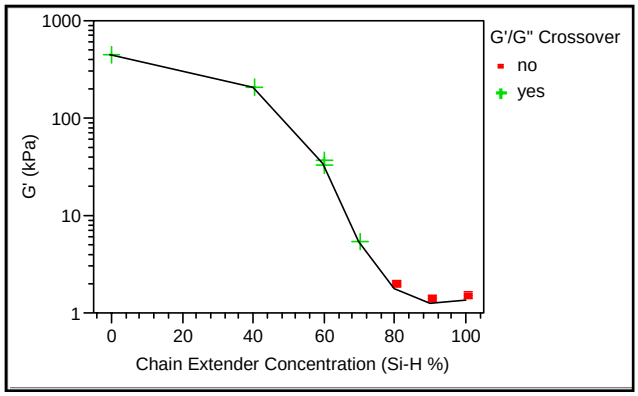

Figure 18: Effect of chain extender concentration on shear modulus

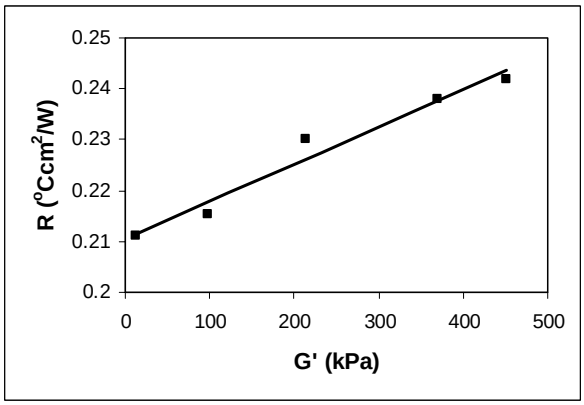

Figure 19: Effect of shear modulus on thermal resistance

Package evaluations of this series of gel TIMs revealed that the thermal resistance in the package decreases with decreasing shear modulus (see Figure 19). Because these formulations have similar bulk thermal conductivities and similar bond line thicknesses, it was hypothesized that the improved resistance is due to reduced interfacial resistance. To test this hypothesis, the gel TIMs were evaluated in a thermal interface tester at several different pressures [30]. It was found that the interfacial resistance to copper blocks decreases with decreasing shear modulus and increasing pressure. Further, the plot in Figure 20 shows that the interfacial resistance results are described by the following empirical equation [31]:

$$\frac{R_c \sigma}{k_{TIM}} = c\left(\frac{G'}{P}\right)^n$$

where σ is the surface roughness, R_c is the contact resistance, k_{TIM} is the bulk thermal conductivity of the TIM, P is pressure, and c and n are empirical coefficients.

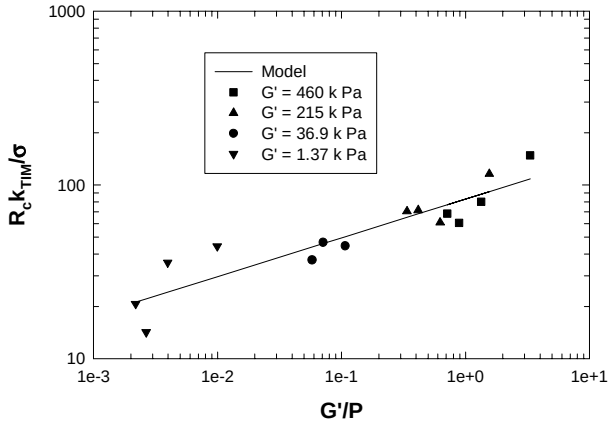

Figure 20: Effect of shear modulus and pressure on interfacial thermal resistance

Packages comprising the gel TIMs were subjected to temperature cycling from 125°C to –55°C, and the thermal resistance was measured after 100 and 350 cycles. The plot of thermal resistance vs. the number of cycles for four of the gel TIMs used in this study is presented in Figure 21. The slope of the data is interpreted to be the degradation rate of thermal performance during temperature cycling. Figure 22 presents a plot of the degradation rate in temperature cycling (determined as described above) vs. the ratio of G'/G" for the entire series gel TIMs. The plot shows that TIM formulations that lack a gel point, such that G'/G" < 1, rapidly degrade during temperature cycling, while gel TIMs with G'/G" > 1 show essentially the same degradation rate during temperature cycling. CSAM analyses revealed that the formulations that lack a G'/G" crossover tend to form voids that are very similar to those observed for grease TIMs due to pump-out. Representative initial and post reliability stress CSAM images of a package comprising a gel TIM with a high concentration of chain extender are presented in Figure 23.

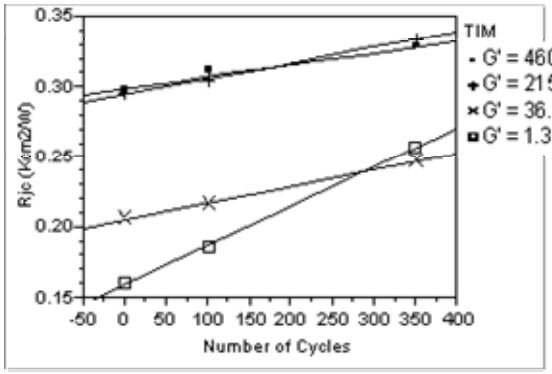

Figure 21: Plot of mean thermal resistance vs. number of temperature cycles. The slopes show the degradation rate of the material during temperature cycling.

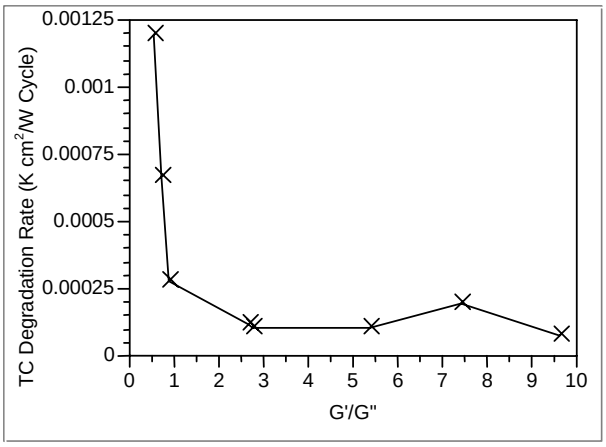

Figure 22: Effect of G'/G" on the degradation rate, as measured by thermal performance of gel TIMs subjected to temperature cycling

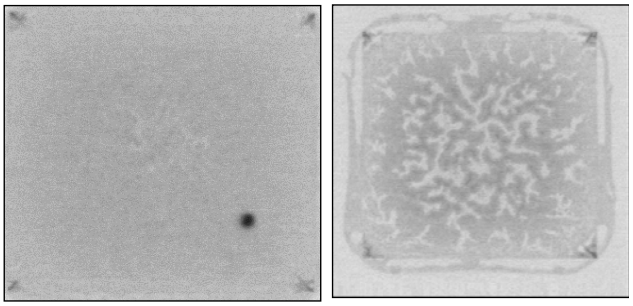

Figure 23: CSAM images before (A) and after (B) reliability stressing showing the development of voids in a gel TIM having G'/G" < 1 by RDA

Based on these results, it is concluded that there exists an optimum range of modulus values for gel TIMs. On the one hand, decreasing the modulus gives decreasing R_{jc} values. However, if the modulus is too low, such that the TIM does not exhibit a gel point, then pump-out can occur during reliability stressing. By optimizing the modulus of the gel TIM using chain extension technology, the R_{jc} target of less than 0.25°Ccm^2/W was achieved both at the end of line and after reliability stressing.

MOLD COMPOUND

A wide variety of electronic package schemes is used to package devices for communication and wireless (C&W) applications [32, 33]. The types of silicon devices used for these applications include memory, logic application processors, and combinations of these devices packaged in a single module. In general, these devices have a much lower die-to-package interconnect count (typically less than 400) than their microprocessor counterparts. The types of packages used in the C&W community have undergone a significant change over the last few decades with a great degree of focus on minimizing the overall

package functionality while reducing package cost [1]. While the semiconductor package industry continues to use many legacy packages for low-end devices, there has been an exponential growth in complex integrated technologies for C&W packages for the purpose of minimizing the overall volume while maximizing the silicon packing density.

The Folded Stacked Chip Scale Package (FSCSP) is a key next-generation package technology that was developed to integrate multiple memory and logic chips into a single module. Figure 24 contains the schematic of the FSCSP package. As seen from the figure, this package technology involves die stacking as well as package stacking. Die stacking is essential to provide high silicon density within a single package, and package stacking is an essential building block technology that provides the capability of stacking multiple types of memory stacks with different logic die packages to enable multiple product designs. A two-metal layer polyimide based "flex" substrate is used for both the top and bottom packages. The bottom package is folded in order to enable package-to-package stacking. Interconnection between the two packages is achieved by the use of solder interconnects. In each of the packages, a die attach process is used to attach the die to the substrate, and to other die in the case of die stacking. Each silicon die is thinned to 3mil (75µm) in order to minimize the overall z-height of the package. Interconnection from the die to the substrate is achieved by gold wirebonds. Each package is then encapsulated with a transfer mold encapsulant. In the case of the bottom package, a folding adhesive material is used to fold the substrate flap and adhere it to the mold surface. This step is essential since it provides a pathway for interconnection between the two packages stacked onto each other.

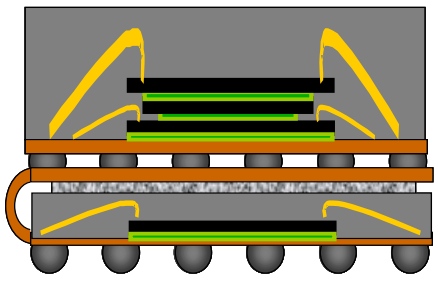

Figure 24: FSCSP schematic

The FSCSP technology presented several materials challenges that were met by developing several new package materials, including flex substrate, film die attach, fold adhesive, and mold compound, all designed for integration with the new flex substrate. The key challenge for the FSCSP mold compound was achieving the tight warpage target of 20 microns, which is required to enable folding and package stacking. Using the current material set, the package warpage (shown in Figure 25) was found to be 50 microns after overmolding and cure, compared to a target warpage of less than 20 microns.

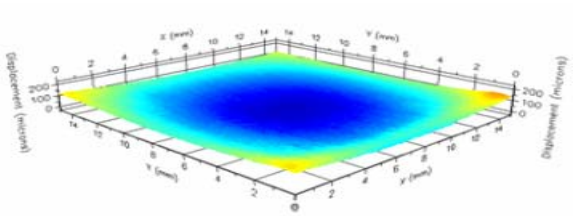

Figure 25: Shadow Moiré measurement of FSCSP bottom package measured at 30ºC showing warparage of 50 microns

It is well known that warpage in a CSP is mainly caused by a CTE mismatch between the different layers of the package. In addition to the choice of materials, the geometric parameters of a package, such as die thickness; mold cap thickness, and die size, also influence package warpage. Package warpage is also influenced by the mold material properties. During assembly, the package goes through multiple high-temperature process steps. An undesirable consequence of these high-temperature exposures compounded with the unavoidable material CTE mismatches (mold compound, thin flexible substrate and silicon die) is package warpage.

Thus, reformulating the molding compound to mitigate warpage was an area of interest vigorously pursued aside from process and design perspectives. The epoxy molding compound selected has a spaced multiaromatic epoxy resin, a known low viscosity, resin. Filler loading in the material was maximized to reduce the CTE and minimize the impact to flow. Given these optimization boundary conditions, the current approach to warpage reduction was to involve the use of flexibilizers as a component in the mold compound, with a previously optimized filler amount in the material. Inclusion of silicone moiety, as a flexibilizer, in the backbone resulted in a decrease in flexural modulus of the cured material at reflow temperatures. Increasing the amount of silicone led to further decreases in the flexural modulus and thus to reduced warpage values as shown in Table 2. However, the high molecular weight silicone species had a drawback of increasing the viscosity of the mold compound as shown in Table 2, thereby posing a risk to wire-sweeping during mold transfer. Therefore, the material was chosen based on a balance between the amount of silicone and the corresponding melt viscosity increase.

Table 2: Different mold compound formulations and properties. Formulation A is the POR material. D has different catalyst type than C.

Molding Compound	A	B	C	D
Melt viscosity at 175(C, Pa.s	5.2	8.2	9.2	9.3
Silicone content	0	1	2	3
Flexural modulus (260(C), N/mm2	1,317	1,130	923	882
CTE-1, ppm/(C	10	10	10	10
CTE-2, ppm/(C	36	40	42	40
Shrinkage, %	0.15	0.10	0.10	0.11
Warpage, microns	50	20	10	12

Once the formulation of the mold compound was frozen at the optimum value, the impact of natural lot-to-lot variation in the mold compound was studied in the Continuous Data Collection (CDC) mode. The transfer molding process was done at 180°C, with an in-mold cure time of 120 seconds and a transfer pressure of 900 psi. The molded strip was subjected to a Post Mold Cure (PMC) of 175°C for four hours to complete the crosslinking reaction. Singulated warpage values were measured by QV404 based on the least square plane of the molded surface.

An analysis of the lots derived from the CDC revealed the warpage correlated with flexural modulus and glass transition temperature (T_g) of the mold compound. All other material parameters had very little impact on the singulated package warpage. The singulated package warpage decreased with an increase in T_g as shown in Figure 26. This may be explained by the fact that the CTE of the material below its T_g (CTE-1) is smaller than the one above T_g (CTE-2). With a higher T_g, the temperature range at which the lower CTE value applies becomes wider. The trend for warpage as a function of room temperature flexural modulus is plotted in Figure 27. As indicated in the figure, the package warpage reduces with the decrease in the flexural modulus.

This study shows that package warpage can be controlled by mold compound material characteristics. The logical approach to warpage reduction for thin package with flexible substrate is to reformulate the molding compound to a lower flexural modulus, increase T_g, and lower CTE. The incorporation of flexible silicone modified epoxy resins into the formulation leads to a reduction in elastic modulus and hence a reduction in warpage.

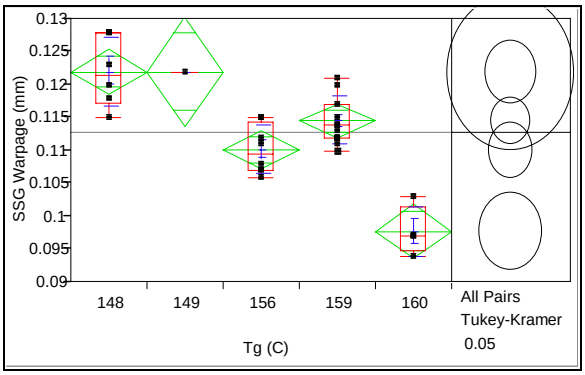

Figure 26: Comparison of singulated warpage vs. T_g variation in mold compound lots

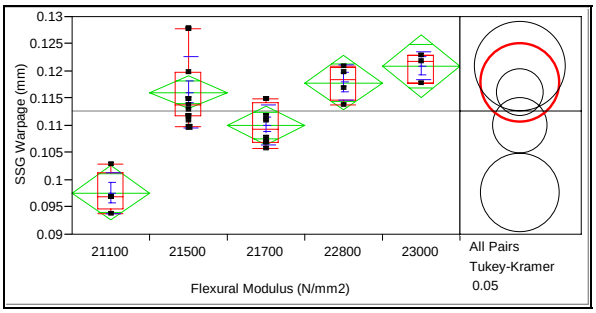

Figure 27: Singulated package warpage as a function of mold compound flex modulus

SUMMARY

Three examples of materials technologies developed to enable low-stress and low-warpage microelectronics packages have been described: (1) first-level interconnect UF and barrier layer metallization for flip-chip packages, (2) TIM for heat removal, and (3) molding compounds for wirebonded dies in a new stacked package form factor. In each case, the key to developing new materials and processing technologies that met the performance requirements was an understanding of the chemistry and the physics of the package materials, and using that understanding to identify the key parameters for modulating performance. This in turn, led to innovation in materials and processes that meet performance requirements.

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